

APPLICATION NOTE

Theory and Application of Sampling Phase Detector

The phase lock of a Voltage Controlled Oscillator (VCO) for VHF, UHF and microwave frequencies is very important in communications and radar application. It combines the far-out phase noise of fundamental oscillators, especially in the microwave frequency range (100 kHz away from carrier frequency and beyond), the excellent long-term stability, and the close-in phase noise of a crystal oscillator (from carrier frequency to 100 kHz away).

A voltage-controlled oscillator can be phase locked by two methods:

1. Digital phase lock: This is usually achieved by using a frequency divider to divide the higher frequency of the VCO to the same frequency of the crystal reference. A digital phase detector is then used to acquire the phase lock. The advantage of this method is that it is self-acquiring and can operate at very low frequencies. It is widely used at low frequencies from 1 MHz up to 3 GHz. However, this method also has two disadvantages. First, the noise floor of the divider will limit its phase noise; and second, at microwave frequencies it will not be economical.
2. Analog phase lock: This is achieved by using an SRD as a comb generator to create a comb of reference frequencies to the frequency of the VCO. The phase detecting is accomplished by using a mixer to detect the phase differences between the reference and the VCO. The Skyworks sampling phase detector is designed to perform the analog phase lock in a simple and more economical way.

The sampling phase detector used in phase lock of a VCO operating by the theory of principles of feedback control systems is shown in Figure 1.

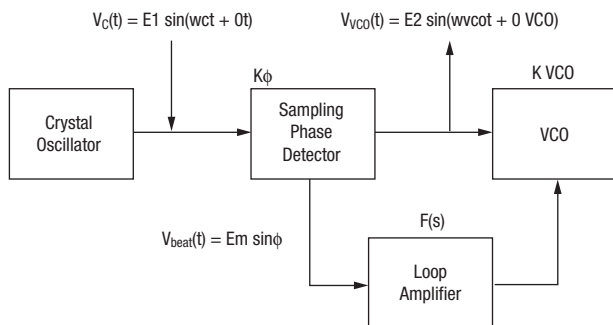


Figure 1.

The error signal output of the sampling phase detector $V_{beat} = E_m \sin\phi$ is the differential phase error between the VCO and the crystal oscillator. The loop amplifier amplifies the error signal to the VCO and corrects the VCO to be in phase with the crystal oscillator. At the same time, the loop amplifier acts as a low pass filter and filters away the crystal frequency.

This method of phase lock will achieve the lowest phase noise possible beside the theoretical degradation of $20 \log N$, where N is the multiplication factor between the crystal oscillator and the VCO. The other circuits that will generate additional noise are the driver amplifier, sampling phase detector, and the loop amplifier. They may all contribute to further degradation in phase noise (typically 1 dB if the crystal oscillator has a noise floor of -155 dBc/Hz or 3 dB if the crystal oscillator noise floor is -160 dBc/Hz).

Circuit Description and Operation of the Sampling Phase Detector

The sampling phase detector is shown in figure 2.

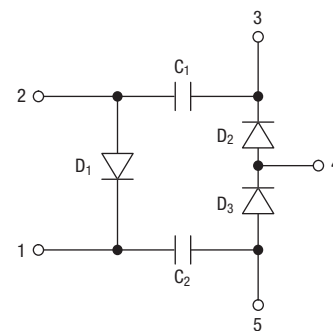


Figure 2.

The sampling phase detector consists of three main parts integrated to form a module. The integrated part has the advantage of minimized size and improved performance, as it eliminates the circuit self-resonance, especially at higher frequencies (13 GHz and above). The following is the description and function of the three parts:

1. SRD: The SRD takes an input crystal frequency and generates a sharp narrow pulse (in the time domain) or combs (in the frequency domain). The period of the pulse is the same as that of the input crystal frequency. The operating range of the sampling phase detector is heavily dependent on the narrow pulse generated by the SRD or the transition time of the SRD. The SRD also needs to recover before the next cycle of the crystal frequency. This is defined by the carrier lifetime of the SRD. Thus, for a selected input crystal frequency and output phase locked VCO frequency, a special SRD is selected in the particular sampling phase detector. There are two ways to optimize the SRD:
 - a) For narrow-band operation, the SRD is selected to optimize at the first peak of $\sin X/X$ wave form, which generates the maximum beat note at a specific frequency.
 - b) For broadband operation, the SRD is selected to 70% of the first null of the $\sin X/X$ wave form, which generates a broad band of combs of virtually equal amplitude. This is more suitable for wide bandwidth operation, as it generates equal beat note over a wide frequency range.
2. Capacitors: The capacitors in the sampling phase detector act as a switch. The switch turns on/off by the pulse generated by the SRD. Therefore, these capacitors should be a single layer microwave capacitor that has very low ESR and high self-resonating frequency well above the operating frequency of the sampling phase detector. The value of the capacitor is typically inversely proportional to the operating frequency. Thus, the higher the operating frequency, the smaller the value of the capacitor. The capacitor controls the efficiency of the transfer of energy or signal from VHF (crystal or multiple frequency) to microwave frequency (VCO). As the capacitor turned "ON," it quickly charged up to its peak RF level, and when turned "OFF," it quickly fully discharged its energy. A more efficient transfer of energy results in lower phase noise.

3. Series pair Schottky diodes: The series pair Schottky diodes in the sampling phase detector are used to detect the errors between the microwave VCO frequency and the crystal reference. The Schottky diodes are turned on and off by the gated capacitor. When turned on, a sample of microwave frequency is compared with the switch frequency. An error frequency proportional to the differences will be generated as an error signal output or beat note. This error signal will be processed through the loop amplifier for phase lock (refer to figure 1). The crucial parameter on the Schottky diodes is the balance between the series pair, especially over temperature. Also, the drive level of the microwave signal sometimes requires medium or high-level Schottky diodes instead of the normal low-level diodes. The drive level should be proportional to the diodes used. Any underdrive results in temperature and unit-to-unit variation. Excessive overdrive will result in increased noise floor. Therefore, the diodes should be selected based on the operation parameter design for them. Skyworks has a variety of sampling phase detectors for all applications.

Characterization and Evaluation of Sampling Phase Detector

There are two circuits widely used to evaluate and characterize the performance of the sampling phase detector. Figure 3a and 3b show the single-end and double-end configuration of the test circuit. These circuits can also be used in real application for phase locked VCO.

To evaluate the sampling phase detector, certain precautions have to be taken to ensure that the data are varied and repeatable. The following is the sequence of setup and test equipment required for the test.

Test Equipment

1. Stable signal source: Crystal oscillators or signal generators. If a signal generator is selected, a synthesized signal generator is preferred.
2. Power amplifier: Frequency range of 10–500 MHz. Capable of 15 dB min. gain and a linear power output of 25 dBm min.
3. Sweep microwave signal generator: Should cover the microwave frequency range to be tested. Power output up to 5 dBm min.
4. Oscilloscope: A dual channel 400 MHz oscilloscope will be adequate for this test.

10 TO 1 TURN RATIO
STEP DOWN TRANSFORMER

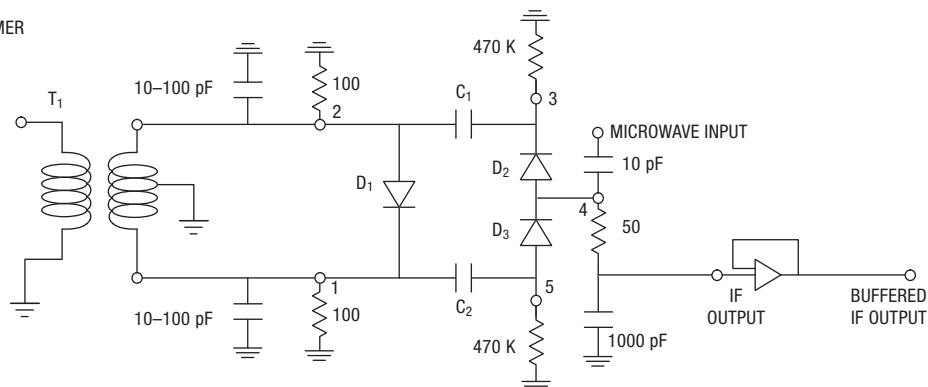


Figure 3a. Test Circuit for Sampling Phase Detector

3 TO 1 TURN RATIO
STEP DOWN TRANSFORMER

REFERENCE INPUT
100 MHz SINE WAVE
+17 to +20 dBm

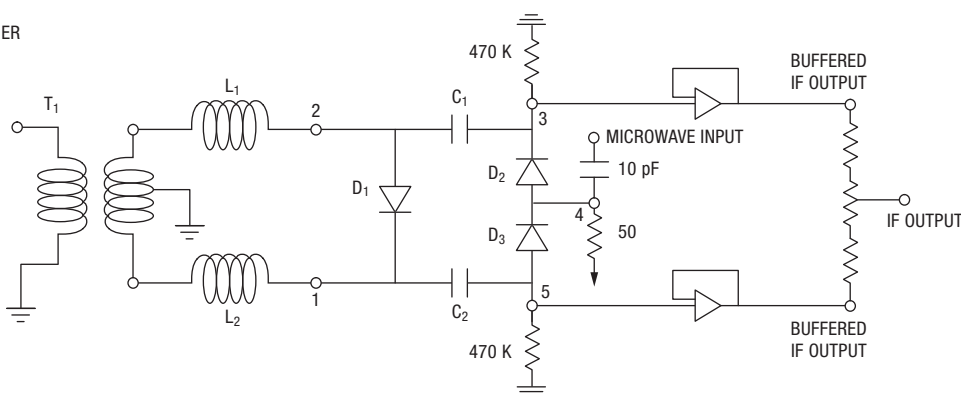


Figure 3b. Test Circuit for Sampling Phase Detector

Test Setup

1. Set up the reference signal, typically 100 MHz @ 17 dBm or 16 V_{pp}, across the primary of the transformer. The reference signal should have minimum harmonic contents.
2. Between the secondary of the transformer and the sampling phase detector is a matching network, which isolates the transformer from the sampling phase detector. The matching network also acts as a termination and tune circuit (Figure 3a) or as a short at reference frequency and an open circuit at microwave frequency. The transformer should have an amplitude balance of 0.5 dB and a phase balance of 2 degrees at the operating frequency of 100 MHz.
3. The microwave signal input is terminated by a thin-film, high-frequency, 50 Ω terminating resistor. The coupling input capacitor acts as a high pass filter, which allows the microwave frequency to pass through, but blocks the lower reference frequency. The beat note output is connecting to the operational amplifier, which is wired as a unity gain buffer. The

operational amplifier is used as a low pass filter and it also lowers the impedance of the Sampling Phase Detector output. As a result, the measured beat note will be consistent and will not be loaded down by the capacitance of the scope probe. The frequency set for the microwave source is the frequency we set to test. The power level of the microwave signal is typically set to 0 dBm.

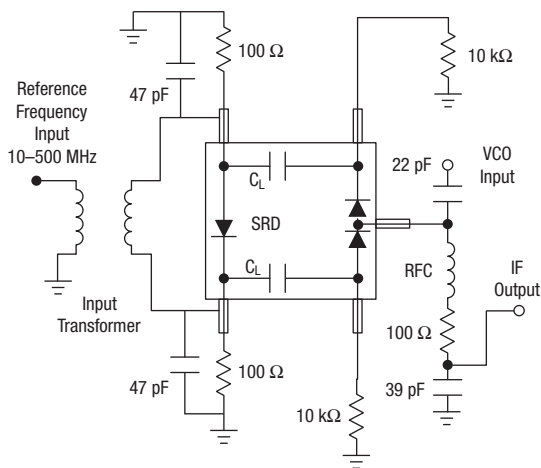
Once all the test conditions are set, the beat note can be measured at the output using the oscilloscope. The input reference signal level and the microwave signal levels are adjusted to measure the 1 dB compression point of the sampling phase detector. The data can be taken across the entire operating bandwidth. Temperature data can be taken in the same manner. From these data, one can select the proper reference frequency and drive level, as well as the proper microwave frequency and power level, which will ensure that their system requirements are met.

Implementation and Optimization of Sampling Phase Detector

To achieve the best phase noise, the implementation and optimization of the sampling phase detector requires the proper selection of the components and circuits. The following are circuit guidelines placed in descending order according to their importance.

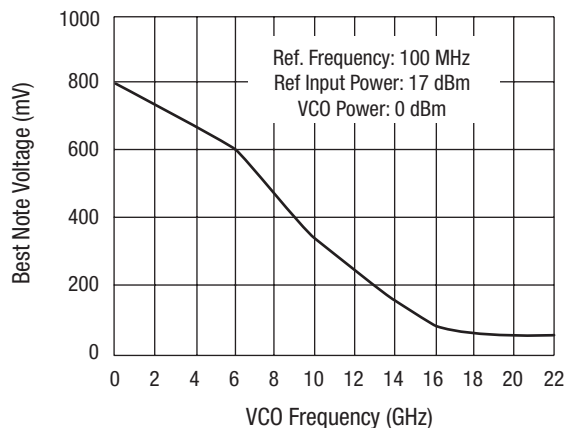
1. The crystal oscillator should have a minimum phase noise of 3 dB better than the system specification from 10 Hz to 100 kHz away from the carrier.
2. The VCO or DRO should have a minimum phase noise of 3 dB worse than the specification at 100 kHz away from the carrier and 6 dB better at 1 MHz away from the carrier. At 5 and 10 MHz away from the carrier, the phase noise should be minimum 3 dB better than the system.
3. The noise loop bandwidth should be set at 250–300 kHz, using a second order loop. This will give enough correction to correct the VCO or DRO phase noise to the crystal reference, and at the same time, suppress the phase noise of the VCO or DRO at 1 MHz.
4. The VCO or DRO should have good tuning linearity. The linear tuning range should be a minimum of twice the range of temperature drift and long-term drift. The linear tuning range defines as the maximum variation of voltage tuning sensitivity by $\pm 10\%$. This will guarantee a stable loop with minimum bandwidth change in temperature.
5. The loop amplifier is also a critical part of the system. A proper operational amplifier should be selected for this function. The operational amplifier should have low noise, low DC offset and low DC offset drift. The bandwidth of the operational amplifier should be between 1–8 MHz. The noise of 2.5 nV/root square Hz is sufficient for most applications. At this level, the operational amplifier is still reasonably priced at about \$1.50 each in 1K quantities. For the extremely low noise of 0.8 nV/root square Hz, the operational amplifier becomes very expensive at approximately \$8.00 each.

Test Circuit and Data on the Sampling Phase Detector



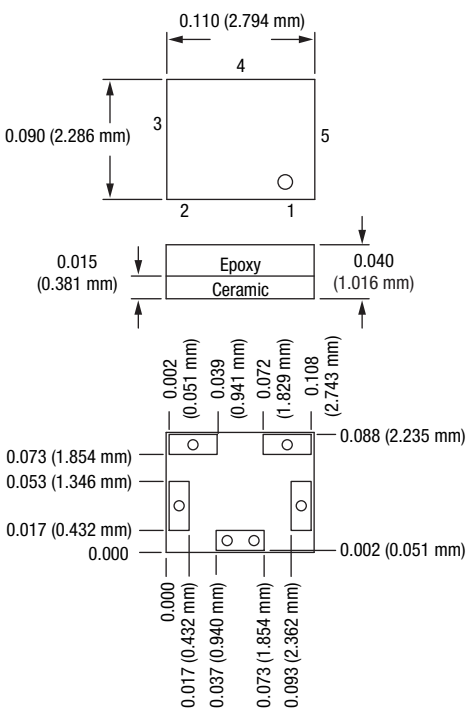
Input transformer: 10:1 step down impedance ratio.

Suggested Circuit

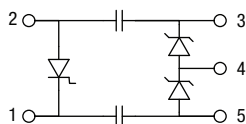


SPD1101-111

Typical Performance



-111 Package Outline



Schematic Diagram

Application of the Sampling Phase Detector

The most widely used application of the sampling phase detector is for phase locking a Dielectric Resonator Oscillator (DRO). The phase-locked DRO is mainly used in the wireless industry, communication systems and RADAR as a stable LO. In all these systems, low cost simplicity, reliability, and good performance are required. Here, we discuss the application of the sampling phase detector used in the function of a phase-locked DRO.

To design a good phase-locked DRO the first requirement is to define the performance of all the components as follows:

1. Crystal oscillator: To ensure the best performance, a 100 MHz 3rd overtone SC-cut crystal is selected to design a crystal oscillator, which can achieve a noise floor of -0.170 dBc/Hz. The cost of the crystal is high, approximately \$20.00 each in 50K quantities. The alternative is to use an AT-cut crystal, which costs approximately \$4.00 each in 50K quantities. However, the trade-off is 3 dB degrading in phase noise and some increase in the long-term aging rate.
2. DRO: The DRO performance is very important. The DRO should have a buffer amplifier to isolate the load pulling and also to achieve an output power of 19 dBm, which is adequate for most applications as LO. The free running phase noise of the DRO at 100 KHz away from carrier should be -116 dBc/Hz minimum over temperature in the operating range (9–13 GHz). The operating range is defined as the linear tuning range of the DRO, which should be twice the temperature drift of the DRO over its operating temperature range. The linear tuning range is defined as the tuning range over which the tuning sensitivity of the DRO varies less than 10%.
3. Sampling phase detector: The sampling phase detector SPD1102-111 will suit for this design.
4. Loop amplifier: For low cost, an Analog Device OP113 will be adequate for the design.
5. Low noise power supply: A low noise power supply is very important for the performance of the phase-locked DRO. In the system, it is preferable to have local, on-board, low noise regulators to supply the voltage source to the individual circuits. This will also isolate the interference from outside and minimize the voltage variation created by current variation and power wire length variation.

In this design, the sampling phase detector circuit we selected is shown in Figure 3b. This was selected because most systems do not have negative voltage available. This allows us to use a single supply and make everything simple and universally adaptable to most systems. The crystal oscillator will be amplified and drive the primary of the transformer with a power level of 16 V peak-to-peak. The DRO/Amp. output is passed through a 16 dB directional coupler. This results in a 2 dBm microwave signal to the sampling phase detector. This will generate a beat note of 400 mV peak-to-peak output. The loop amplifier used is a second-order loop (Figure 4a), and the phase noise loop bandwidth was set at 300 kHz.

A wide loop bandwidth will be less susceptible to microphonics. This is very important in the wireless industry, as the unit is normally mounted outside and is subject to such environmental effects as wind, rain and hail. In this configuration, we can achieve a system phase noise of -80 dBc/Hz at 100 Hz; -104 dBc/Hz at 1 kHz; -114 dBc/Hz at 10 kHz; -124 dBc/Hz at 100 kHz; -136 dBc/Hz at 1 MHz; -155 dBc/Hz at 5 MHz. The system noise floor limits the phase noise measurement at 5 MHz on the HP Phase Noise Measurement System. If further suppression of noise is required, a higher order of loop amplifier design can be selected as shown in Figures 4b through 4d.

The simplicity of the sampling phase detector used in the phase-locked DRO allows us to fabricate the complete circuit including the reference crystal oscillator all on one small PC board. The integration of the high-frequency components into one single package allows us to eliminate wire-bonding, and as a result, create a complete system which can be automated using surface mount technology.

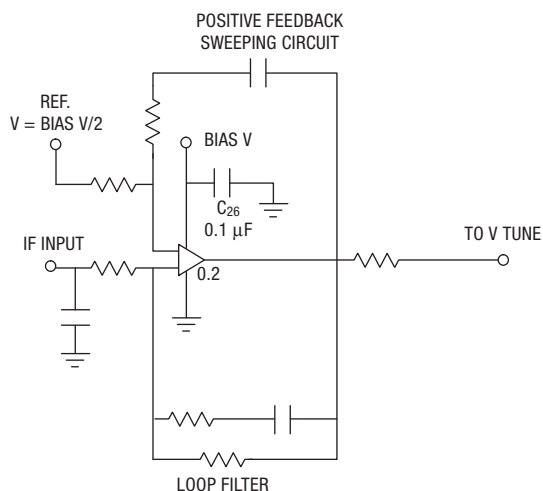


Figure 4a. Second-Order Loop

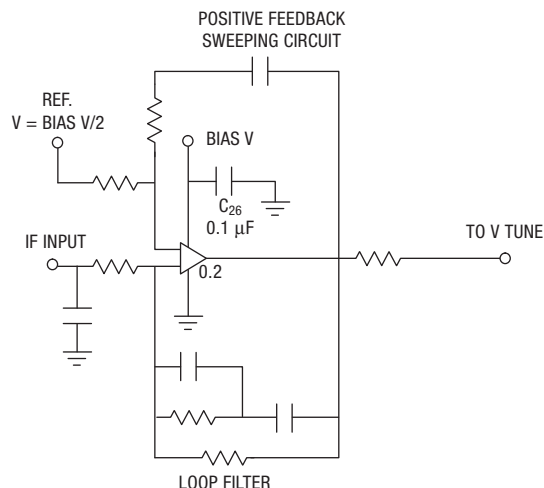


Figure 4b. Third-Order Loop

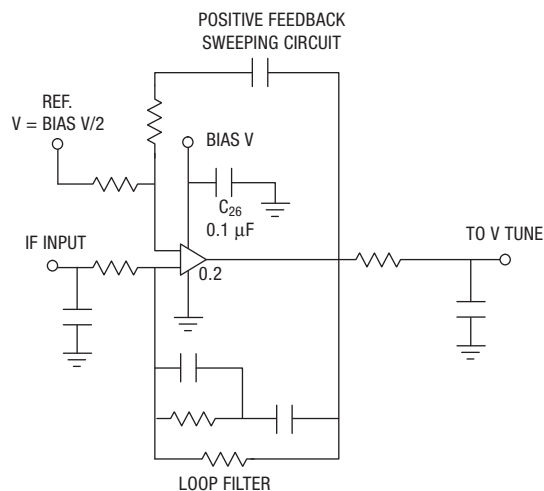


Figure 4c. Fourth-Order Loop

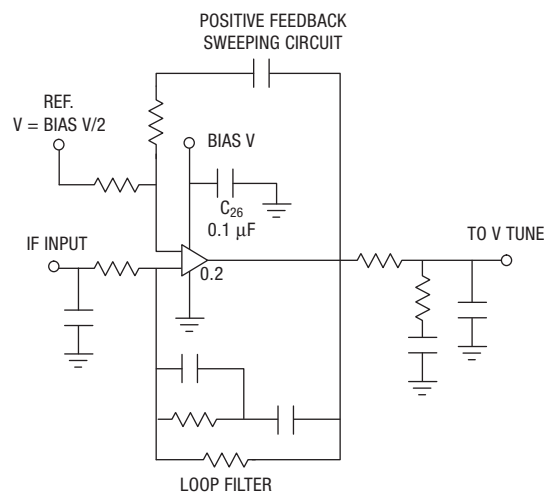


Figure 4d. Fifth-Order Loop

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