

APPLICATION NOTE

Depletion Mode pHEMT Bias Networks

Introduction

Skyworks provides standalone GaAs pHEMTs that require external bias and RF matching networks to realize their best performance. Parameters such as gain, Noise Figure (NF), and linearity are controlled by the pHEMT's bias point. This Application Note describes the many ways to properly bias a pHEMT and outlines the performance characteristics for each circuit.

pHEMT Bias Conditions

Both the gate and drain of a pHEMT must meet bias conditions to function properly. The drain voltage relative to the source (V_{DS}) should be ≥ 2 V, while the gate voltage relative to the source (V_{GS}) is used to set the current flow from the drain to the source (I_{DD}). Figure 1 shows the basic circuit representation of a pHEMT.

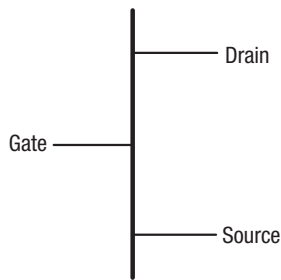


Figure 1. Basic pHEMT Circuit Representation

With $V_{GS} = 0$ V and $V_{DS} \geq 2$ V, the FET is in its saturated state (I_{DSS}) and draws the maximum amount of current. The value of I_{DSS} is determined by the overall geometry and size of the pHEMT. Lowering V_{GS} to approximately -0.7 V, the device enters its pinchoff state and turns off. Typical IV characteristics of a Skyworks 200 μ m FET is illustrated in Figure 2.

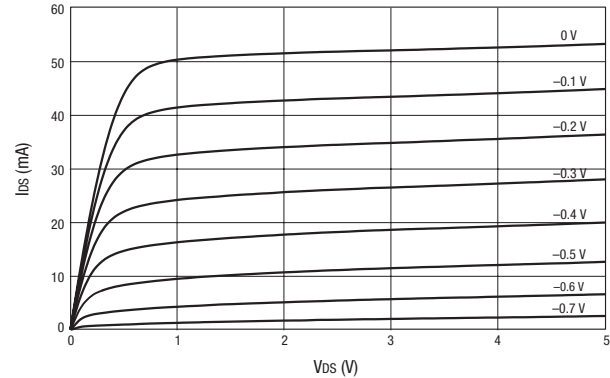


Figure 2. Typical IV Characteristics for a 200 μ m pHEMT

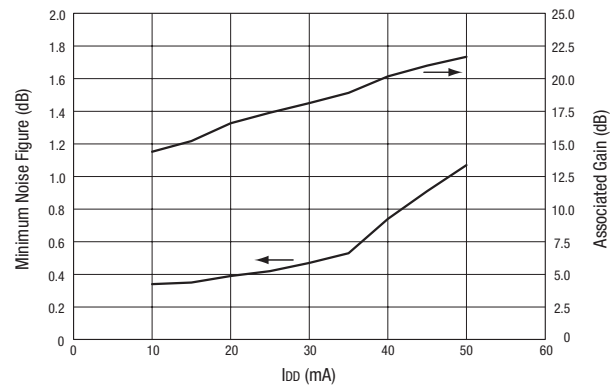


Figure 3. Minimum NF and Associated Gain vs I_{DD} for a 200 μ m pHEMT

Performance Considerations

The bias point chosen for a pHEMT largely controls the performance parameters such as NF, gain, and linearity. Figure 3 illustrates how noise and gain are affected by the I_{DD} . For applications in which noise is the most important specification, the pHEMT should be biased around 20 percent of the I_{DSS} value or, in this case, 10 mA. Increasing I_{DD} increases gain and linearity, but at the expense of an increased NF.

A 200 μ m pHEMT such as the SKY65050-372LF is ideal for low power and low noise applications in which linearity is not a critical specification. If the NF and linearity are both important, a larger device such as the SKY65053-377LF should be considered. This 400 μ m device has an I_{DSS} of 100 mA, which allows it to be biased at a higher I_{DD} point and still maintain a low NF performance.

Bias Circuits

The bias networks shown in Figures 4 and 5 illustrate the two most common ways to bias pHEMTs. Circuit A uses a positive drain voltage (V_D) and a negative gate voltage (V_G) to set the quiescent point of the device. This circuit provides low noise, high gain, and high efficiency. The circuit offers the best performance, but requires a negative voltage supply, which can increase overall component cost and layout area.

To eliminate the need for a negative voltage supply, a self-biasing resistor is placed between the source of the device and ground. The source is floated above ground when current flows through the resistor. The source resistor simplifies the bias network design, but also has a few caveats. The resistor slightly degrades NF performance and the added source bypass capacitor can cause oscillations. The characteristics of both circuits are summarized in Table 1.

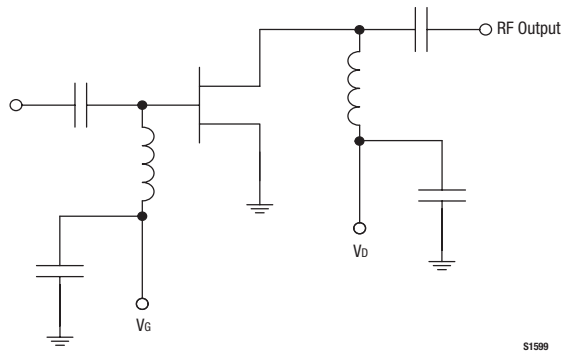


Figure 4. pHEMT Circuit A: Gate and Drain Biased Separately

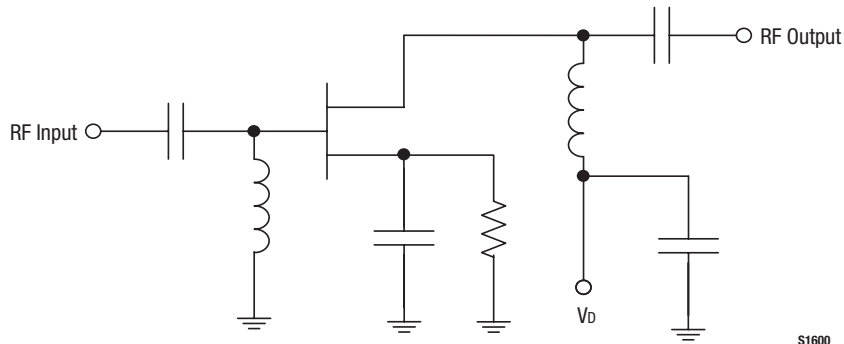


Figure 5. pHEMT Circuit B: Single DC Supply Operation

Table 1. pHEMT Circuit Summary

Circuit (See Figures 4 and 5)	Circuit Characteristics	Power Supply
A	Low noise High gain High efficiency	Positive and negative supply
B	Low noise High gain Lower efficiency Gain and current are adjusted with external resistor	Positive supply

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